IEEE EPTC 2023

Singapore | Dec 5-8, 2023

25th Electronics Packaging Technology Conference

IEEE EPS Flagship Conference in the Asia and Pacific Region

2nd Call for Registration

ABOUT EPTC

The 25th IEEE Electronics Packaging Technology Conference (EPTC2023) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapters and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputable international electronics packaging conference and is the IEEE EPS flagship conference in the Asia and Pacific Region. It aims to cover the complete spectrum of electronic packaging technology. Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation, and AI. EPTC2023 will feature keynotes, technical sessions, invited talks, panels, workshops, exhibitions, and networking activities.

The EPTC technical program committee, with more than 100 experts from diverse semiconductor packaging technology areas, is committed to creating an engaging technical program for the international packaging community. The technical program will be supplemented by an exhibition, which provides an opportunity for leading companies to exhibit their latest technologies and products. Last year there were 430 attendees. This year being our 25th Anniversary, we have a special 4-day program and expect more attendees.

CONFERENCE TOPICS

Research publication covered the below major conference topics

1. Advanced Packaging
2. TSV/Wafer Level Packaging
3. Interconnection Technologies
4. Emerging Technologies
5. Materials and Processing
6. Assembly and Manufacturing Technology
7. Electrical Simulation & Characterization
8. Mechanical Simulation & Characterization
9. Thermal Characterization & Management
10. Quality, Reliability & Failure Analysis
11. Advanced Optoelectronics and Displays
12. Smart Manufacturing & Equipment Technology

CONFERENCE VENUE:

Grand Copthorne Waterfront Hotel, Singapore

CONFERENCE REGISTRATION SCHEDULE

Early Bird Registration	**October 31, 2023**
Standard Registration	December 5, 2023

Please click here for conference registration and click here for hotel booking.

CONFERENCE FEE DETAILS

Category	Membership	Early Bird Rate	Standard Rate
Authors/ co-authors/ Speakers	IEEE	S$900	S$1100
	Non-IEEE	S$1000	S$1200
Attendees	IEEE	S$1100	S$1200
	Non-IEEE	S$1200	S$1400
Students	NA	S$600	S$700
PDC Only	Regular	S$400	S$500
	Student	S$200	S$250
Full Conference included 1 PDC Group registration discount available for registration pax ≥ 5 delegates. For more information, please contact the Secretariat			

Please check the conference website for the latest updates.

BEST PAPER AWARDS

The best oral papers from Academia, Industry and Students will receive cash awards and certificates. A best interactive paper award will also be presented. More details are available on the EPTC website.

CALL FOR EXHIBITORS

Details of the exhibition opportunities are available on the ***conference website***. For enquiries, please email exhibition@eptc-ieee.net.

STUDENT TRAVEL GRANTS

To encourage students in the electronics packaging field to become members of EPS and actively participate in the flagship conferences of the society, up to 6 Student Travel Grants will be offered for EPTC annually. Also, to widen the representation of female students and students from underrepresented countries, at least two grants will be allocated to female student authors and one to a student from a country historically underrepresented at EPTC. Please find details on the EPTC website.

AFFILIATE MEMBERSHIP SUBSIDY PROGRAM

To encourage EPS membership and engagement with EPS, EPS has initiated an Affiliate Membership Subsidy Program whereby non-member conference registrations at EPTC and the other two EPS flagship conferences will be offered a complimentary EPS Affiliate Membership for the following year.
Please find details on the EPTC website.

If you have questions about presentations, registration and payment, please send your queries to secretariat@eptc-ieee.net

The following events are currently confirmed but may be changed due to unforeseen circumstances.

Keynote Talks

Advanced System Integration Technology Trend

Abstract:
HPC and AI/ML technologies have a profound impact on human society. Semiconductor technology plays a critical role in realizing these. Recently progress in generative AI drives AI/ML's impact to a new height. Higher performance computing with ever-increasing model size requires much higher level of computation performance, communication, and memory bandwidth, all at higher energy efficiency (EE). Advanced nodes Si scaling is expected to continue providing higher performance computing with higher EE. Advanced heterogeneous system integration technologies, however, can provide even more values than before for the HPC and AI/ML systems. This can be achieved by the scaling up of classical(microelectronics)-based system integration, advanced photonics-based system integration, as well the two integrated.

Speaker's Biography

Dr Douglas Yu is a Vice President of TSMC R&D and TSMC Distinguished Fellow responsible for system integration technology pathfinding. Previously Doug led TSMC Cu/Low-K technology development and established industry's first wafer level system integration technology platform TSMC 3DFabricTM including CoWoS®, InFO and SoICTM. These technologies start new semiconductor technology trends and set industry standards. Doug also pioneered TSMC COUPE (Composite Universal Photonic Engine), a photonics integration technology. Prior to TSMC, Doug worked with AT&T Bell Labs. He received Ph.D. degree in Materials Engineering from Georgia Institute of Technology, Atlanta, GA. Dr. Yu received the IEEE Rao Tummala Award, the IEEE EPS Microelectronics Manufacturing Award, and the President Science Prize, Taiwan. He is an IEEE Fellow and a member of the National Academy of Engineering. Doug has made numerous invited/keynote/plenary speeches in international conferences and published over 150 papers to elevate the profile of system integration technology.

2.5D/3D Heterogeneous Integration for Silicon Photonics Engines

Abstract
As, per lane, data rates continue to rise, optical interconnects are getting closer and closer to the processor to minimize overall system power consumption. To this end, to design what is essentially a processor with optical IO, higher levels of integration are needed to build optical engines. We will discuss various integration approaches that have been taken to accomplish very compact optical interconnect systems.

Speaker's Biography

Dr. Radha Nagarajan is Senior Vice President and Chief Technology Officer of Marvell's Optical and Copper Connectivity Group. In this role, he manages the development of the company's optical platform technology and products. Radha joined Marvell from Inphi, where he served as the Senior Vice President and Chief Technology Officer of Platforms. Prior to joining Inphi, he was a Fellow at Infinera where he was focused on the design, development, and commercialization of large scale photonic integrated circuits. Dr. Nagarajan has been awarded more than 230 US patents and is a Fellow of the IEEE, Optica (formerly OSA) and IET (UK). He was awarded the 2006 IEEE/LEOS Aron Kressel Award and the 2022 IPRM Award in recognition of breakthrough work in the development and manufacturing of large scale photonic integrated circuits. He holds a B.Eng. from the National University of Singapore, M.Eng. from the University of Tokyo, and Ph.D. from the University of California, Santa Barbara, all in Electrical Engineering.

Advanced Packages Enriching Heterogeneous Integration

Abstract
Advanced IC Packages are typically Ball Grid Array (BGA) and Flip-Chip (FC) based with various structures to meet demanding high performance chiplet computing needs. This presentation will discuss innovative BGA, Fan-Out with FC technologies – FOCoS, plus 2.5D / 3D packages, describing how the integration needs are optimized with higher precision, effective layout with enhanced electrical signal and power performance, very essential for new generation AI server, data center, 5G and latest edge computing applications.

Speaker's Biography

Dr. C.P.Hung currently holds the position of Vice President, Corporate R&D, at ASE Group. Based in Taiwan, he leads teams responsible for next-generation product development featuring integrated technologies, as well as a broad range of advanced chip, package, and system integration solutions. During his tenure, Dr. Hung has performed a variety of management roles at ASE, including VP of Corporate Design, VP of Central Engineering & Business Development and VP of Logistic Services Integration. He holds 180 patents encompassing IC packaging structure, process, substrate, and characterization technology. He has also published over 105 conference and journal papers. Dr. Hung has been the SEMICON Taiwan PKG & TEST Committee Chair since 2013, and currently Co-Chair since 2021. He is also a member of the IEEE EPS Board of Governor since 2019.

Will Advanced Packaging Save Moore's Law?

Aabstract

Dimensional scaling in leading edge logic technology is becoming increasingly challenging. This presentation will review critical issues associated with logic technology and examine system and technology co-optimization as a viable path to extend Moore's law through adoption of advanced packaging technology. We will discuss fundamental equipment capabilities that must be established in the coming years to enable true 3D integration of chiplets.

Speaker's Biography

Dr. Yang Pan joined Lam Research in 2003 and is currently Corporate Vice President focusing on defining and enabling of technology and product roadmap for advanced packaging. He was the head of Advanced Technology Development group and Global Product Group CTO in Lam Research headquarter. He was also the head of Lam Research China from 2003 to 2014. Before joining Lam, he held various positions at Chartered Semiconductor Manufacturing Ltd from 1994 to 2003, including Vice President of Fab3 and Fab1 operations, GM of Silicon Manufacturing Partners (SMP), and process integration and device engineering manager in the Research and Development Group. Yang Pan received his Ph.D. degree in Electrical Engineering from Delft University of Technology, the Netherlands. He was a technical committee member of VLSI Technology Symposia. He was an adjunct associated professor at National University of Singapore. He received Lee Kuan Yew Postdoctoral Fellowship from National University of Singapore in 1992. Yang Pan has been awarded more than 60 U.S. patents and published more than 40 papers in international journals and conferences.

Panel Sessions

Chiplet Integration

Moderator: Dr. Jiantao Zheng, Huawei

Panelists:

- Dr. Ravi Mahajan, Intel Fellow and Director of Pathfinding for Assembly and Packaging Technologies, Intel.
- Dr. Chih.Pin.Hung, Vice President, Corporate R&D, ASE Group;
- Dr. Arvind Sundarrajan, Managing Director/ Head of Applied Packaging Development Center, Applied Materials.
- Dr. Surya Bhattacharya, Director of System in Packaging, Institute of Microelectronics, A*STAR Singapore.

Artificial Intelligence for Package Design and Manufacturing

Moderator: Dr. Sam Karikalan, Broadcom Inc., Vice President of Conferences - IEEE EPS

Panelists:

- Dr. Byung Joon Han, Chief Executive Officer, Silicon Box, Singapore.
- Ms. Grace O'Malley, Vice President Technical and Project Operations, iNEMI;
- Mr. Vincent DiCaprio Vice President, Applied Materials.
- Prof. Kuo Ning Chiang, National Tsing Hua University.

Technology Talk

Challenges in the Analysis and Testing of Advanced Packaging Systems

Abstract
Demands for miniaturization, whether driven by the need for portability or the need to integrate more functionality into a small form factor, is leading to higher levels of integration. Although there are many advantages of 2.5D and 3D packaging structures, there are also many challenges arising for their testing and analysis. These advanced performance-driven designs create further challenges for packaging, testing, and thermal management. One of the challenges is the feature size and operating speed of these devices which are now sub-micron, where traditional methods of thermal analysis such as infrared thermography are no longer adequate. Some failures are embedded inside 3D structures, and it is a challenge to establish their location within the structures. For advanced microwave systems such as Antennae-in-Package (AiP), beam-steering and beamforming antennas, characterization of their electromagnetic fields is a challenge due to the partial and spatial coherence of the resulting fields. This presentation will describe the above-mentioned challenges and techniques available to meet these challenges including thermal characterization of sub-micron microelectronic and photonic devices, electromagnetic field characterization of advanced microwave systems, and failure analysis of heterogeneously integrated devices.

Speaker's Biography
Dr. Mo Shakouri is co-founder, President & CEO of Microsanj LLC, a leading supplier of high resolution, thermal imaging systems designed to address the thermal challenges faced by today's advanced device designers. Dr. Shakouri received his PhD from Stanford University and has more than 20 years of experience directing major programs with Hewlett-Packard Corporation, Lucent Technologies, and Alvarion Corporation prior to the founding of Microsanj in 2007. Mo also serves as CEO for Telewave.io which designs and manufactures high quality products for RF networks. Telewave.io strives to be the premier supplier of seamless interoperable communication systems that provide security and reliability in mission critical eco-systems for both commercial and military applications worldwide. Mo is also the Board Chairman for the WiMAX Forum which is an industry trade organization formed by leading communications, component, and equipment companies to promote and certify compatibility and interoperability of broadband wireless access equipment that conforms to the IEEE 802.16 and ETSI HIPERMAN standards.

List of Invited Papers (To be Updated)

Forward-Looking Roadmap View to Enable Heterogeneous Integration in the Next 10 Years, **Gamal Refai-Ahmed**, AMD, USA
Development of Novel Polymer Materials for Advanced Packaging, **Takenori Fujiwara**, Toray, Japan

Fluxless Bonding for Higher Density & Bandwidth Packaging, **Steve Ng**, KnS

Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Advanced Interconnects, V. Dragoi, EVG, Germany

Die-to-Wafer Hybrid Bonding to Address Next-Gen Electronics Packaging Challenges, Avi Shantaram, Applied Materials, USA
Signal and Power Integrity Performance of CoWoS-R in Chiplet Integration Applications, Chuei-Tang Wang, TSMC, Taiwan
The Era of Generative AI and Advanced Packaging, Chak Wing Kei, Tommy, ASMPT, Hong Kong

Professional Development Courses

Fan-Out, Chiplet, and Heterogeneous Integration Packaging

Course Objective:

There are two parts of this lecture: First part of the course convers the Fan-out and chiplet design for 1 hour followed by second part of course covers the Heterogeneous integration packaging for 2 hours. For fan-out, the following topics will be presented and discussed: (1) Fan-out wafer/panel-level Packaging; (2) Formation of FOWLP, (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First); (3) Fabrication of Redistribution Layers (RDLs), (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu Damascene + CMP, (c) Hybrid RDLs, and (d) Laser drill + LDI + PCB Cu-plating + Etching; (4) Formation of FOPLP, (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First); (5) TSMC InFO, (a) InFO-PoP, and (b) InFO_AiP Driven by 5G mmWave; (6) Samsung WLP/PLP, (a) PoP for Smart Watches and (b) SiP SbS for Smartphones; (7) Warpages, (a) Warpage Types and (b) Allowable of Warpages; (8) Reliability of FOWLP and FOPLP, (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations; and (9) Examples, (a) Chip-First Panel-Level Fan-Out Packaging of Mini-LED for RGB-Display, (b) Chip-Last Panel-Level Fan-Out Packaging of Application Processor Chipset, (c) 2.3D IC Integration with Chip-First Fan-Out RDL-Interposers, and (d) 2.3D IC Integration with Chip-Last Fan-Out RDL-Interposers. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. For fan-in packaging, a six-side molded wafer level package and its reliability will be presented. The trends of fan-out and fan-in wafer-level packaging will be discussed. Chiplet is a chip design method and heterogeneous integration is a chip packaging method. Chiplet design and heterogeneous integration packaging have been generated lots of tractions lately. For the next few years, we will see more implementations of a higher level of chiplet designs and heterogeneous integration packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption.

Course Outline:

(1) System-on-Chip (SoC) and Why Chiplet Design?
(2) Chiplet Design and Heterogeneous Integration Packaging:
    a. Chip partition and Heterogeneous Integration
    b. Chip split and Heterogeneous Integration
    c. Advantages and Disadvantages
(3) Lateral Communication between Chiplets (e.g., Bridges):
    a. Bridge Embedded in Build-up Package Substrate
    b. Bridge Embedded in Fan-Out EMC with RDLs
    c. UCIe
    d. Hybrid Bonding Bridge
(4) Chiplet Design and Heterogeneous Integration Packaging:
    a. Multiple System and Heterogeneous Integration with Package Substrate (2D IC Integration)
    b. (Multiple System and Heterogeneous Integration with Thin Film layer on the Package Substrate (2.1D IC Integration)
    c. Multiple System and Heterogeneous Integration with TSV-less (Organic) Interposer (2.3D IC Integration)
    d. Multiple System and Heterogeneous Integration with Passive TSV-Interposer (2.5D IC Integration)
    e. Multiple System and Heterogeneous Integration with Active TSV-Interposer (3D IC Integration)
(5) Summary
(6) Potential R&D Topics in Chiplet Design and Heterogeneous Integration Packaging.

Who Should Attend?

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. Each attendee will receive more than 300 pages of lecture notes.

Instructor's Biography

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging has published more than 515 peer-reviewed papers (375 are the principal investigator), 40 issued and pending US patents (25 are the principal inventor), and 23 textbooks (all are the first author) such as Fan-Out Wafer-Level Packaging (Springer, 2018), Heterogeneous Integration (Springer, 2019), Semiconductor Advanced Packaging (Springer, 2021). and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

Flip Chip Interconnect by Eric Perfecto

Course Objective:
This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various type of wafer bumping technologies, solder joint formation, non-solder joints and assembly considerations. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today's flip chip assembly. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, etc. Special focus of the course will be on fine pitch technologies, mainly u-Pillar and Hybrid bonding.

Course Outline:
- Introduction to Flip Chip Technologies
- Flip Chip Technologies: Mass Reflow vs Thermal Compression Bonding
- Packaging Technologies
- Bumping Ground Rules
- Flip Chip Under-Bump Metal and Intermetallic
- Flip Chip Solder Deposition Processes
- Cu Pillar Technology
- Hybrid Bonding

Who Should Attend:
The goal of this course is to provide the students with a comprehensive understanding of flip chip fabrication and its use on the various advanced packages. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions.

Instructor's Biography

Eric Perfecto has over 40 years of experience working in the development and implementation of C4 and advanced Si packages at IBM and GlobalFoundries. Eric's responsibilities include UBM and Pb-free solder definition for C4 and u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College. Eric has published over 80 external papers, including two best Conference Paper Awards and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 60 US patents and has been honored with three IBM Outstanding Technical Awards. Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. Eric is an IEEE Fellow, an EPS Distinguish Lecturer and EPS VP of Education.

Co-Packaged Si Photonics: Opportunities and Challenges

Course Objective and Outline:
This course will overview the tools, technologies and approaches which enable Si photonics to empower the co-packaged optics initiatives pursued by the industry presently. The capabilities offered by existing Si photonics dictate, to a large extent, the advantages offered by co-packaged optics to the CMOS eco-system. Abilities for co-packaged topics to positively fuel scaling system in a package (SiP) by enhancing the interconnection density will be used as an example in this course.

This comprehensive course aims to provide a thorough exploration of the fundamental tools, cutting-edge technologies, and innovative approaches that underpin the remarkable potential of Silicon (Si) photonics in driving and supporting the ongoing co-packaged optics initiatives within the current industry landscape. As the industry places increasing emphasis on co-packaged optics as a strategic direction, understanding the intricacies of Si photonics becomes pivotal, as its capabilities and functionalities wield a significant influence over the advantages that co-packaged optics can bring to the broader CMOS ecosystem.

Who Should Attend:
The goal of this course is to provide the participants with a multifaceted analysis of Si photonics, examining its foundational principles, engineering intricacies, and diverse applications. By grasping the core attributes of Si photonics, course participants will gain a profound insight into the pivotal role it plays in shaping the co-packaged optics landscape. One noteworthy aspect that will be highlighted is how the inherent capabilities of Si photonics serve as a linchpin for the advantages conferred by co-packaged optics. This relationship will be elucidated through illustrative examples, such as the way co-packaged optics can significantly augment the scalability of Systems in Package (SiP) through heightened interconnection density. Through a systematic exploration of these interconnected concepts, participants will not only foster a comprehensive understanding of Si photonics and co-packaged optics but also develop a discerning perspective on how these elements synergistically contribute to the evolution of modern packaging technologies. By the course's conclusion, attendees will be equipped with not only theoretical knowledge but also practical insights that can be harnessed in real-world scenarios, enabling them to make informed decisions and innovations in the dynamic realm of co-packaged optics and Si photonics. As the industry landscape continues to be shaped by rapid advancements, this course stands as an

invaluable resource for those seeking to navigate the intricate interplay between Si photonics and co-packaged optics, ultimately empowering them to drive forward advancements in system integration, interconnectivity, and performance optimization.

Instructor Biography:

Amr S. Helmy is a professor in the department of electrical and computer engineering at the University of Toronto. Prior to his academic career, Amr held a position at Agilent Technologies - UK, between 2000 and 2004. At Agilent his responsibilities included developing lasers and monolithically integrated optoelectronic circuits. He received his Ph.D. and M.Sc. from the University of Glasgow with a focus on photonic integration technologies, in 1999 and 1995 respectively.

His research interests include photonic device physics, with emphasis on plasmonic nanostructures, nonlinear and quantum photonics addressing applications in information processing / sensing, and data communications. Amr is an active volunteer and leader of the IEEE Photonics Society, currently serving as an Elected Member of the Society's Board of Governors and as a Distinguished Lecturer. He was also the recipient of the Society's 2019 Distinguished Service Award.

Design-on-Simulation Technology for Advanced Packaging Reliability Life Prediction

Course Objective and Outline:

The electronic packaging (EP) community has widely used Design-on-Simulation (DoS) technology for designing a new packaging structure. Still, it has encountered some challenges in ensuring a trustable simulation result. AI/machine learning approaches can be combined with DoS to solve this uncertainty. This course will use wafer-level packaging (WLP) to illustrate the solution methodology and procedure, including the FE model, mechanics theories, controlled mesh size validation, large database generation, and AI training performance of different machine learning algorithms. This talk will also describe how to combine AI and finite element simulation to estimate the reliability life of wafer-level packaging and obtain the best structure combination of each packaging component. This course will cover the following topics: (1) Finite element simulation, (2) 2D/3D model, (3) Material constitutive equations, (4) Mesh size control concept, (5) Simulation theory/materials/model validation procedure, (6) Solder joint reliability life cycle prediction empirical equations, (7) AI-Assisted DoS.

Who Should Attend:

This course aims to provide students and engineers with a comprehensive understanding of how to properly combine mechanics theories, constitution equations of material, finite-element modelling, and reliability life prediction empirical equations to estimate the reliability life cycle of area array type advanced packaging. Attendees are encouraged to bring topics and technical issues from their past, present, and future job functions for group discussions.

Instructor Biography:

Professor K. N. Chiang received his PhD from the Georgia Institute of Technology, USA. He is the Chair Professor at the National Tsing Hua University in Hsinchu, Taiwan. After graduating from Georgia Tech, he worked four years as a senior researcher at MSC/NASTRAN, a world-famous finite element system. From 2010 to 2013, he served as General Director of the National High-Performance Computing Center, which is the National Strategic Research Center of Taiwan. He has received outstanding research awards from the Ministry of Science and Technology of Taiwan three times and has published more than 450 technical papers in international journals and conference proceedings. He has been granted more than 50 invention patents. Among the major awards Professor Chiang received are the Excellence in Mechanics Award from ASME (2022) and the Outstanding Sustained Technical Contribution Award (2020) from IEEE-EPS. Currently, he is Editor-in-Chief of the Journal of Mechanics (SCI), Academic Editor of Materials (SCI), and Associate Editor of the Journal of Electronic Packaging (SCI). He is an IEEE, ASME, STAM, and IMAPS Fellow. And an academician of the International Academy of Engineering (IAE).

He has made significant achievements in simulation-based science and technology. He successfully combined simulation design with artificial intelligence technology and applied it effectively to semiconductor-related designs. His technology has greatly reduced product development time and development costs. He has worked with many major electronic packaging, semiconductor and LED companies such as ACET, TSMC, MediaTek, UMC, EPISTAR, VIA, Powertech Technology, etc.

Automotive Electronics Reliability – Challenges and Opportunities

Course Objective and Outline:

The modern car has increased semiconductor content and dollar value. Semiconductors enable the majority of innovations in automotive. The increased emphasis on autonomous driving and the electrification of vehicles has resulted in enormous changes for semiconductors and packaging. The design, materials, and reliability strategies for automotive electronics will be presented. Electronics are increasingly being used in automotive platforms for various mission-critical and safety-critical activities, such as guidance, navigation, control, charging, sensing, and operator interaction. Over the last two decades, automotive platforms have expanded to incorporate hybrid and fully electric vehicles. Much of the electronics is located under the car's hood or in the trunk, where temperatures and vibration levels are far higher than in consumer office applications. During the vehicle's use-life, electronics in the automotive underhood may be exposed to sustained high temperatures of 125-150°C for extended periods. The Automotive Electronics Council (AEC) has graded electronics for automotive purposes into four categories: grade 0, grade 1, grade 2, and grade 3. Grade-0 components have the most demanding criteria of the four grade categories, with predicted power temperature cycling ranging from -40°C to +150°C for 1000 cycles and ambient temperature cycling ranging from -55°C to +150°C for 2000 cycles. Furthermore, the grade-0 components are expected to be capable of sustaining high-temperature storage for 1000 hours at 175°C. With the introduction of new packaging architectures, packaging applications have continued to evolve, allowing for powerful computing on mobile automobile platforms. New materials and integration technologies have also emerged, allowing for tighter integration of electronics sensing and processing into the structural characteristics of the vehicle. The automobile platform faces a series of constraints particular to the real-time context for enabling sophisticated functionality.

Specifically, the course will encompass the following topics:

1. Role of electronics on the automotive platform
2. Automotive environments
3. Zero-Defects
4. Second-Level Solder Interconnect Design Considerations
5. Copper Wirebond Interconnects
6. Advanced Packaging Interfaces
7. Vibration Effects
8. Sustained High Temperature and Wide Thermal Extremes
9. Corrosion Propensity
10. Accelerated Testing

Who Should Attend:

The goal of the course is to provide the students with a comprehensive understanding of the materials and reliability considerations in the design of electronics for operation in the automotive platform. The course is intended to have an intermediate degree of difficulty to serve as an introduction for engineers and managers looking to design electronics for operation in the automotive underhood.

Instructor Biography:

Pradeep Lall is the MacFarlane Endowed Distinguished Professor and Alumni Professor with the Department of Mechanical Engineering. He is the Director of the NSF-CAVE3 Electronics Research Center at Auburn University. He holds Joint Courtesy Appointments in the Department of Electrical and Computer Engineering and the Department of Finance. He is a member of the technical council and academic co-lead of automotive TWG and asset monitoring TWG of NextFlex Manufacturing Institute. He is the author and co-author of 2-books, 15 book chapters, and over 900 journal and conference papers in the field of electronics reliability, manufacturing, safety, testing, energy efficiency, and survivability. Dr. Lall is a fellow of the ASME, a fellow of the IEEE, a Fellow of NextFlex Manufacturing Institute, and a Fellow of the Alabama Academy of Science. He is a recipient of the SEMI Flexi R&D Achievements Award for landmark contributions to Additive Printed Electronics, ASME Avram Bar-Cohen Memorial Medal, IEEE Biedenbach Outstanding Engineering Educator Award, Auburn University Research Advisory Board's Advancement of Research and Scholarship Achievement Award, IEEE Sustained Outstanding Technical Contributions Award, NSF-IUCRC Association's Alex Schwarzkopf Award, Alabama Academy of Science Wright A, Gardner Award, IEEE Exceptional Technical Achievement Award, ASME-EPPD Applied Mechanics Award, SMTA's Member of Technical Distinction Award, Auburn University's Creative Research and Scholarship Award, SEC Faculty Achievement Award, Samuel Ginn College of Engineering Senior Faculty Research Award, Three-Motorola Outstanding Innovation Awards, Five-Motorola Engineering Awards, and over Forty Best-Paper Awards at national and international conferences. Dr. Lall is the founding faculty advisor for the SMTA student chapter at Auburn University and a member of the editorial advisory board for SMTA Journal.

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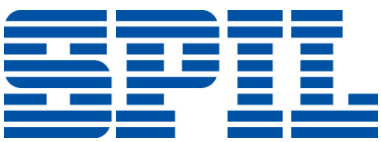

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